#### **REMARKS**

Applicants amend claims 1-3, 6-9, 11, 13-15, 18, 22, 27-28, 30-32, and cancel claim 29. No new matter is added. Applicants note with appreciation that the Examiner deems claims 7-11, 14, 15, 18-27, 30, and 31 to recite allowable subject matter. Claims 1-28, 30-32 are presented for examination, of which claims 1, 18, and 28 are independent. For the reasons set forth below, Applicants respectfully submit that claims 1-28, 30-32 define over the art of record.

# Objections to the Drawings

The Examiner objects to the Drawings for some minor issues. Applicants respectfully submit that the Drawings are amended to address the Examiner's concerns.

The Examiner objects to the Drawings because of non-legible reference numbers.

Applicants subsequently amend the Drawings to include formal reference numbers.

The Examiner further objects to the Drawings because the Examiner suggests that the Drawings do not show every feature of the invention specified in the claim. Specifically, the Examiner request that the first receiver stage and the second receiver stage of the first and second receivers must be shown or the features canceled from the claims. Applicants hereby amend the drawings to include a first and second receiver as limited by claim 3. Applicants respectfully submit that claim 3 does not include the limitation of a first state and a second stage as stated by the Examiner. Applicants respectfully submit that the amended Drawings together with amended claim 3 show features of a first receiver stage and the second receiver stage of the first and second receivers, which is mentioned in several places in the Specification. No new matter is added.

The Examiner further requested that the integration amplifier of the second stage of the first receiver as well as the integration amplifier of the second stage of the second receiver must be shown as claimed in claim 6 or the features canceled from the claim. Applicants hereby amend claim 6 to recite the synchronous interconnect structure comprising an integration amplifier. Applicants respectfully submit that amended claim 6 now correspond to the drawings. No new matter is added.

# **AMENDMENTS TO THE DRAWINGS**

The attached sheet(s) of drawings includes changes to Figure 1—3.

Attachment:

Replacement sheet

Annotated sheet showing changes

The Examiner further request that the delayed locked loop circuit must be shown as claimed in claim 14 or the features canceled from the claim. Applicants hereby amend the Drawings to include the feature of a delayed locked loop circuit, which is mentioned in the Specification in several places. Applicants also amend claim 14 to clarify the invention. No new matter is added.

In view of the amendments set forth above, Applicants respectfully request the Examiner to reconsider and withdraw the objections to the Drawings.

#### Objections to the Claims

Claims 1-32 are objected by the Examiner for minor informalities. Applicants have made several claim amendments to address the Examiner's concerns. Applicants respectfully request the Examiner to reconsider and withdraw the objections to the claims.

#### Rejection of Claim 13 Under 35 U.S.C. §112

Claim 13 is rejected under 35 U.S.C. §112, second paragraph, as indefinite. Applicants amend claim 13 to address the Examiner's concern. Applicants respectfully request the Examiner to reconsider and withdraw the objections to the claims in view of the amended claim 13.

#### Rejection of Claims 1, 2, 28, 29 and 32 Under 35 U.S.C. §102

Claims 1, 2, 28, 29, and 32 are rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent No. 6,801,592 to Christensen (hereafter Christensen). To establish a prima facie case of anticipation, each and every element and limitation of the present invention must be disclosed expressly or inherently in a single prior art reference. Applicants respectfully submit that Christensen does not disclose each and every element of amended independent claims 1 and 28.

The claimed invention provides a synchronous interconnect structure for communication between a first integrated circuit and a second integrated circuit. The synchronous interconnect structure provides an approach to compensate for the timing alignment amongst one or more

data or clock signals traveling from the first integrated circuit to the second integrated circuit. Both the data signal and the clock signal are delayed by a delay circuit, where a phase locked loop circuit provides a time varying signal that indicates when the amount of the propagation delay should be inserted into the data and clock signals and the amount of delay is based on an output signal of a detection circuit.

Claim 1 is amended to recite the limitation of a control circuit to control an amount of a propagation delay inserted into a first transmission path and a second transmission path, wherein a data signal propagates on a first transmission path and a source clock signal propagates on a second transmission path.

Christensen shows a delay flip flop (D-FF) in Fig. 1-3. However, these flip flops only delay the data signal and does not delay a clock signal. The amended claim 1 now require that an amount of a propagation delay is inserted into a first transmission path and a second transmission path, wherein a data signal propagates on the first transmission path and a source signal propagates on the second transmission path. Therefore, Christensen does not disclose each and every element of independent claim 1.

Claim 28 is amended to recite a delay circuit delaying both a first data signal and a course clock-signal based on an output signal of a detection circuit. As set forth above, Christensen only shows a delay of a data signal and never shows a delay of a click signal. Therefore, Christensen does not disclose each and every element of independent claim 28.

Claims 2 and 32 depends on independent claims 1 and 28 respectively and includes all the limitation of the corresponding independent claim. Therefore, Christensen does not disclose each and every element of claims 2 and 32. Claim 29 is canceled. Therefore, the rejection of claim 29 is moot. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejections of claims 1-2, 28, and 32.

# Rejection of claims 3-6 under 35 U.S.C. §103

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen in view of United States Patent No. 6,396,888 to Notani et al. (hereafter Notani). To establish a

prima facie case of obviousness, the prior art references, either alone or in combination, must teach or suggest each and every limitation of the rejected claims. Applicants respectfully submit that Christensen and Notani, either alone or in combination, do not teach or suggest each and every limitation of claims 3-6.

Claims 3-6 depend on claim 1 and include all the limitations of claim 1. As set forth above, Christensen does not disclose the limitation of an amount of propagation delay inserted into a first transmission path and a second transmission path, wherein a data signal propagates on the first transmission path and a source clock signal propagates on the second transmission path, as recited by amended claim 1. Applicants respectfully submit that Christensen does not teach or suggest this limitation. Christensen only uses delay flip flops, which only delays a data signal. Additionally, flip flop can only be used to store one bit of data, but the claimed invention uses transmission lines which carries multiple bits to data. Therefore, Christensen does not teach or suggest the limitation of an amount of propagation delay inserted into a first transmission path and a second transmission path, wherein a data signal propagates on the first transmission path and a source clock signal propagates on the second transmission path, as recited by amended claim 1. Claims 3-6 also include this limitation of claim 1, and Christensen does not teach or suggest it. Applicants further submit that Notani fails to cure the deficiency of Christensen.

Notani discusses a system for transmitting digital data, a frame pulse signal and a clock signal. However, no where does Notani teach or suggest an amount of propagation delay inserted into a first transmission path and a second transmission path, wherein a data signal propagates on the first transmission path and a source clock signal propagates on the second transmission path, as required by claims 3-6.

As set forth above, Christensen and Notani, either alone or in combination, does not teach or suggest each and every limitation of claims 3-6. Applicants respectfully request the Examiner to reconsider and withdraw the rejections of claims 3-6.

### Rejection of claims 12, 16, and 17 under 35 U.S.C. §103

Claims 12, 16, and 17 are rejected under 35 U.S.C. as being unpatentable over Christensen in view of Unites States Patent No. 4,755,704 to Flora et al. (hereafter Flora).

Applicants respectfully submit that Christensen and Flora, either alone or in combination, does not teach or suggest each and every limitation of claims 12, 16, and 17.

Claims 12, 16, and 17 depend on independent claim 1 and include all the limitation of claim 1. As set forth above, the arguments made regarding Christensen's failure to teach or suggest the limitation of an amount of a propagation delay inserted into a first transmission path and a second transmission path, wherein a data signal propagates on the first transmission path and a source clock signal propagates on the second transmission path, as recited by claim 1, apply with equal force here and are reiterated as if set forth in full. Applicants respectfully submit that Flora fails to cure the deficiency of Christensen.

Flora discusses an apparatus for providing automatic clock deskewing for a plurality of circuit boards of a data processing system. However, Flora only concerns of deskewing of the clock signal and does not teach or suggest an amount of a propagation delay inserted into a first transmission path and a second transmission path, wherein a data signal propagates on the first transmission path and a source clock signal propagates on the second transmission path, as required by claims 12, 16, and 17.

Accordingly, Christensen and Flora, either alone or in combination does not teach or suggest each and every limitation of claims 12, 16, and 17. Applicants respectfully request the Examiner to reconsider and withdraw the rejections of claims 12, 16, and 17.

## **CONCLUSION**

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Applicants believe no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-067 from which the undersigned is authorized to draw.

Dated: April 20, 2005

Respectfully submitted,

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Attachments

Docket No.: SMQ-067

DESKEWING ARCHITECTURE

**ANNOTATED SHEET** 



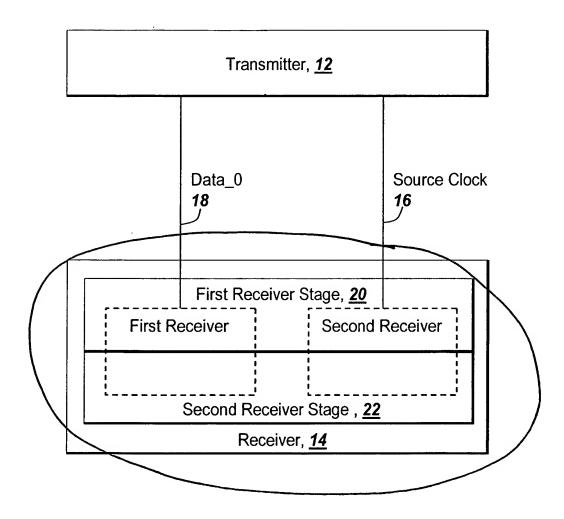


Fig. 1

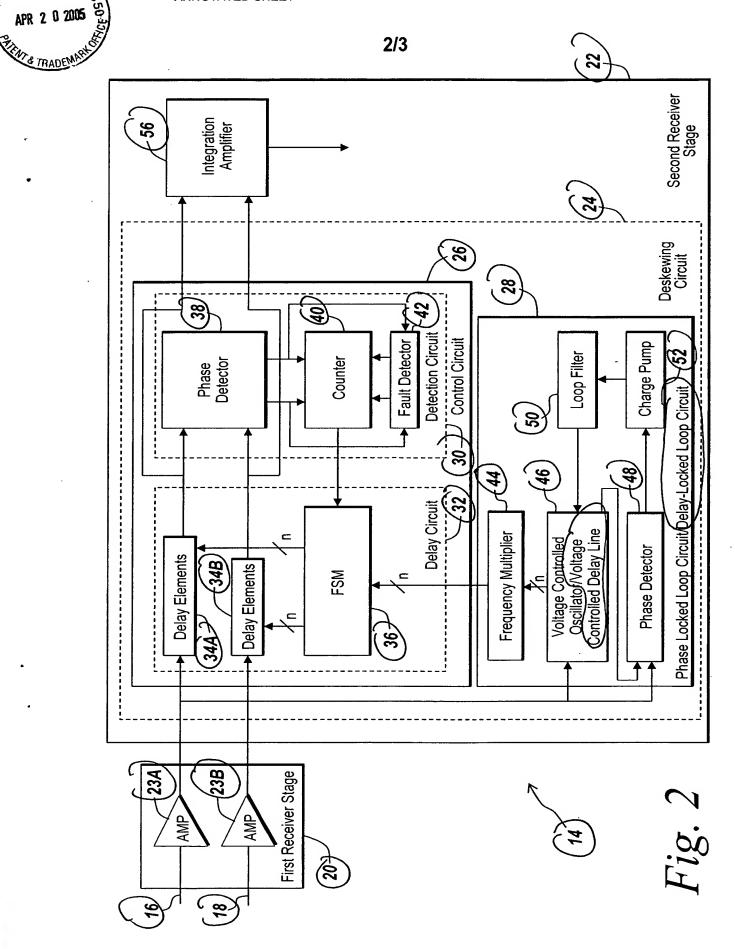
App No.: 10/016196 Docket No.: S Inventor: Hiep P. NGO et al. Title: SINGLE-ENDED IO WITH DYNAMIC SYNCHRONOUS

Docket No.: SMQ-067

**DESKEWING ARCHITECTURE** 

OIP

ANNOTATED SHEET



APR 2 0 2005

Title: SINGLE-ENDED IO WITH DYNAMIC SYNCHRONOUS

DESKEWING ARCHITECTURE

ANNOTATED SHEET



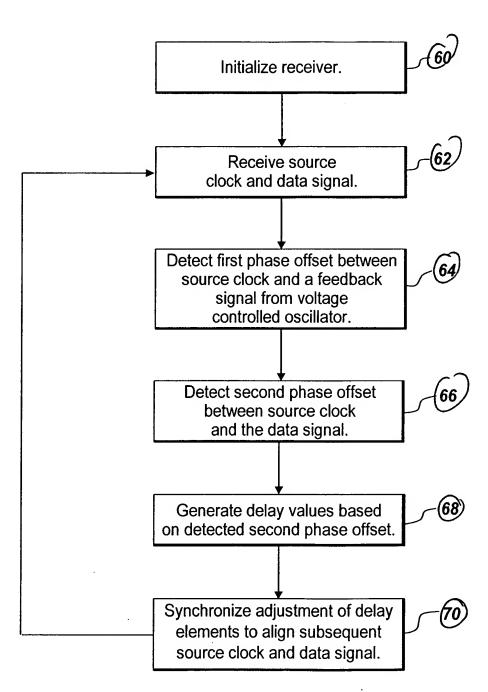


Fig. 3